1. A data storage system wherein a host computer is coupled to a bank of disk drives through an interface, such interface having a plurality of directors and a memory interconnected by a four busses, such directors controlling data transfer between the host computer and the bank of disk drives as such data passes through the memory, such interface comprising:

(A) a printed circuit board having:

(a) a plurality of electrical connectors arranged in a linear array and electrically connected to the busses, such electrical connectors being adapted to receive director printed circuit boards having the directors and the memory printed circuit boards having the memory, and electrically interconnect the directors and the memory received therein to the busses;

(b) wherein a front end portion of the directors are coupled between the host computer and the busses through a front end portion of ESCON adapters and a back end portion of the directors are coupled between the bank of disk drives and the busses through the back end portion of the adapters;

(c) wherein each one of such adapter boards comprises:

(i) a plurality of adapter ports each one being coupled to a corresponding port of the host computer;

(ii) a plurality of adapter board gate arrays;

(iii) a plurality of optic interfaces, each one being coupled between a corresponding one of the adapter port and a corresponding one of the adapter board gate arrays, wherein each coupled optic interfaces and gate array provides a corresponding one of a plurality of independent channels for the data, the plurality of channels being adapted to pass data concurrently therethrough.

2. The system recited in claim 1 wherein the memory comprises a plurality of memory sections each one having different addresses of the memory, each one of the memory sections being received in a corresponding one of the electrical connectors and being electrically connected to a corresponding one of a pair of the four busses, one of the memory sections being electrically connected to a first bus of

the first pair of busses and a second bus of the second pair of busses and the other one of the memory sections being electrically connected to a second bus of the first pair of busses and a first bus of the second pair of busses.

3. The system recited in claim 2 wherein each one of the directors is electrically connected to the plurality of memory sections through the busses.

4. A data storage system wherein a host computer is coupled to a bank of disk drives through an interface, such interface comprising:

a plurality of directors;

a bus;

a memory connected to the directors through the buss;

wherein the directors control data transfer between the host computer and the bank of disk drives as such data passes through the memory;

a plurality of ESCON adapters, a front end portion of the directors being coupled between the host computer and the busses through the ESCON adapters; wherein each one of such adapters includes:

a plurality of adapter ports each one being coupled to a corresponding port of the host computer;

a plurality of adapter board gate arrays;

a plurality of optic interfaces, each one of the optic interfaces being coupled between a corresponding one of the adapter port and a corresponding one of the adapter board gate arrays, each one of the coupled optic interfaces and gate array providing a corresponding one of a plurality of channels for the data.

5. The system recited in claim 4 wherein each adapter also comprises:

a plurality of adapter board CPUs, each one being coupled to the adapter board gate arrays and the optic interface of a corresponding one of the channels, each one of the CPUs controlling the initiation and termination of the data passing through said corresponding one of the channels.

6. The system recited in claim 5 wherein each one of the front end portion of the director boards includes a plurality of director board gate arrays and a plurality of EDACs; and

wherein each pair of the director board gate arrays is coupled between a corresponding pair of the adapter board gate arrays and a corresponding one of the EDACs.

7. The system recited in claim 6 including a plurality of director board CPUs each one is coupled to a corresponding one of the adapter board CPUs, each one of the director board CPUs being coupled to a corresponding one of the director board gate arrays to control the initiation and termination of a data transfer through such coupled one of the director gate arrays.

8. The system recited in claim 7 including a common state machine coupled to the plurality of director gate arrays and the plurality of EDACs for arbitrating between the pair of director gate arrays coupled to the corresponding one of the EDACs for access to such corresponding one of the EDACs.

9. The system recited in claim 8 wherein each one of the directors comprises: a plurality of dual port RAMs, each one being coupled to a corresponding one of the EDACs and to at least one of the busses; and, a second common state

machine coupled to the first common state machine and the plurality of dual port RAMs for arbitrating between the plurality of dual port RAMS for access to one the at least one of the busses.